

APPLICATION NOTE

Phase Noise Performance of the SKY72300, SKY72301, and SKY72302 Dual Synthesizers/PLLs

This Application Note describes the total output phase noise performance of a Phase Locked Loop (PLL) using Skyworks SKY72300, SKY72301, and SKY72302 dual synthesizers.

Phase Noise Contributors in a PLL

In any oscillator, the intention is to generate a single tone sine wave that has constant amplitude and frequency. In a real application, assuming the amplitude is constant, there would appear random spectral components caused by thermal noise, 1/f noise of transistors, and the finite Q of a resonant circuit. These random spectral components can be collectively viewed on a spectrum analyzer as phase noise.

The total output phase noise of a PLL is determined by three factors:

- Crystal oscillator phase noise
- Synthesizer phase noise
- Voltage-Controlled Oscillator (VCO) phase noise

Step Size

The SKY72300, SKY72301, and SKY72302 synthesizers achieve their step size by using a $\Delta\Sigma$ fractional-N modulator. As a result of this, there are some differences in calculating total phase noise compared to the techniques applied to integer-N synthesizers. This document describes these differences to fully appreciate the impact that step size has on the total phase noise of a PLL.

The SKY72300 and SKY72301 synthesizers feature 18-bit fractionality on the main synthesizer portion, which gives a resolution of 262144 steps with respect to the internal reference frequency. The SKY72302 features a 16-bit resolution. These step sizes are related to the internal reference and not to the output frequency, which means that the 1.0 GHz PLL or the 2.1 GHz PLL have the same step size.

The formula for computing the step size is:

$$\text{Step size [in Hz]} = \left(\frac{F_{xtal}}{R} \right) \left(\frac{1}{2^{18}} \right)$$

where: $R = \frac{F_{xtal}}{F_{ref}}$

Example 1:

Using a 20 MHz crystal and a reference division of $R = 1$,

$$\text{Step size} = \left(\frac{20}{1} \right) \left(\frac{1}{262144} \right)$$

$$\text{Step size} = 76.29 \text{ Hz}$$

This represents the minimum step size achievable with a 20 MHz crystal oscillator and $R = 1$.

Example 2:

Using a 20 MHz crystal and a reference division of $R = 32$:

$$\text{Step size} = \left(\frac{20}{32} \right) \left(\frac{1}{262144} \right)$$

$$\text{Step size} = 2.38 \text{ Hz}$$

This represents the minimum step size achievable with a 20 MHz crystal oscillator and $R = 32$.

The 2.38 Hz and 76.29 Hz step sizes represent the minimum and maximum values when using a 20 MHz crystal and 18-bit resolution. The difference is due to selecting a different value of R to set the internal reference frequency.

In an integer-N synthesizer, the crystal reference is divided by an integer number to achieve an internal frequency equal to the step size. In these conventional dual modulus loops, the step size is a result of the VCO being divided down in frequency by a prescaler that only produces integer divisions. The net result is that the step size is equal to the reference frequency at the phase detector. Therefore, the divide ratio can be integers such as 46, 47, 48, etc.

In a $\Delta\Sigma$ -based synthesizer, the prescaler is modulated in a statistical fashion to realize division ratios that are not restricted to integers. An 18-bit $\Delta\Sigma$ fractional-N synthesizer can make the resolution 262144 finer in step size. In other words, there are 262144 steps between 46 and 47, etc.

There are differences generating the step size between an integer-N and fractional-N synthesizer. These differences affect the resulting value of N in a PLL.

Example 3:

Calculate the value of N in a 900 MHz integer-N PLL to generate a 6.25 kHz step size using a 20 MHz crystal.

Step size in an integer-N PLL is determined by:

$$\text{Step size} = \left(\frac{F_{xtal}}{R} \right)$$

$$6.25 \text{ kHz} = \left(\frac{20 \text{ MHz}}{R} \right)$$

$$R = 3200$$

This means that the crystal frequency has been divided by 3200 to achieve a step size of 6.25 kHz.

In an integer-N PLL, step size is also equal to the internal reference frequency. Therefore, the internal reference frequency is also 6.25 kHz.

To calculate N , use the following equation:

$$N = \left(\frac{F_{out}}{F_{ref}} \right)$$

$$N = \left(\frac{900 \text{ MHz}}{6.25 \text{ kHz}} \right)$$

$$N = 144000$$

Therefore, an integer-N synthesizer PLL with an output of 900 MHz and a step size of 6.25 kHz has N equal to 144000.

Example 4:

Calculate the value of N in a 900 MHz PLL using the SKY72301 fractional-N synthesizer to generate a 6.25 kHz step size using a 20 MHz crystal.

As shown in Example 1, the resulting step size is 76.29 Hz, which exceeds the 6.25 kHz specification by 82 times ($R = 1$ means that F_{ref} is equal to F_{xtal}). To calculate N , use the following equation:

$$N = \left(\frac{900 \text{ MHz}}{20 \text{ MHz}} \right)$$

$$N = 45$$

Therefore, using the SKY72301 fractional-N synthesizer to generate a 900 MHz output with a 76 Hz step size means that N is 45.

As a result, the integer-N PLL needed a large N value of 144000 to achieve the required 6.25 kHz step size, where the 18-bit fractional-N PLL only needed N to be 45 while achieving a 76 Hz step size.

When using the Skyworks synthesizers in fractional-N mode, it is recommended that a crystal reference frequency of less than 25 MHz be divided down only to achieve extremely fine resolution (refer to the Synthesizer Phase Noise section below). This will ensure a superior performance with respect to phase noise.

Reference division is required when a crystal frequency between 25 and 50 MHz is used, in which case the crystal frequency must be divided down to 25 MHz or less by choosing a value of $R = 2$. This ensures that the final value of the internal reference frequency is below the maximum of 25 MHz.

Crystal Oscillator Phase Noise

The dominant close-in phase noise contributor to the total phase noise is the crystal oscillator phase noise multiplied by the division ratio of N/R , which relates the internal reference back to the crystal frequency.

$$20 \log \frac{N}{R}$$

where: $N = \frac{F_{out}}{F_{ref}}$

Example 5:

Calculate the added phase noise for a 20 MHz crystal in a PLL operating at 920 MHz with $R = 1$ (which reduces the formula to $20 \log [N]$).

$$\text{Added phase noise} = 20 \log \left(\frac{920 \text{ MHz}}{20 \text{ MHz}} \right)$$

$$\text{Added phase noise} = 33 \text{ dB}$$

Therefore, the additional phase noise contribution of 33 dB is added to the original phase noise of the crystal.

Example 6:

Using the 33 dB additional phase noise, calculate the resultant phase noise of the crystal at a 10 kHz offset where the original crystal oscillator phase noise was -130 dBc/Hz at the 10 kHz offset.

$$-130 \text{ dBc/Hz} + 33 \text{ dB} = -97 \text{ dBc/Hz}$$

Therefore, measured at 10 kHz offset from the carrier, the multiplied phase noise contribution of a 20 MHz crystal that has a -130 dBc/Hz phase noise brings the total phase noise of a 920 MHz synthesizer PLL to -97 dBc/Hz .

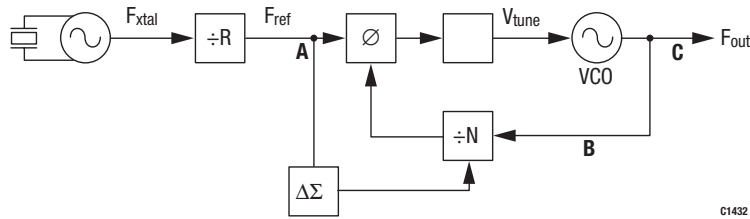


Figure 1. PLL Synthesizer Loop

The calculations in the previous examples involved the use of an external crystal oscillator. The SKY72300, SKY72301, and SKY72302 synthesizers have an integrated internal crystal oscillator that operates at up to 50 MHz and has a phase noise floor of -130 dBc/Hz. The internal reference frequency (F_{ref}) has a maximum of 25 MHz.

Crystal phase noise contributions are typically greater in PLL systems with a small step size using integer-N synthesizers. In this case, the internal reference of the synthesizer is divided down significantly to achieve a very fine step size.

When the crystal frequency is multiplied up, the phase noise increases by $20 \log(N)$. However, when the crystal frequency is divided down as occurs when R is greater than 1, the divided down internal reference frequency (F_{ref}) also has the phase noise decreased at the same rate of $20 \log(N)$. This means that if F_{ref} has been divided down from F_{xtal} , the phase noise seen at F_{ref} has a better phase noise than that of the original crystal.

Example 7:

Calculate the crystal phase noise contribution at the VCO output to the total phase noise of a PLL when N equals 144000 (as in Example 3), $R = 1$, and the phase detector noise floor equals -150 dBc/Hz.

$$VCO \text{ output phase noise} = -150 \text{ dBc/Hz} + 20 \log(144000)$$

$$VCO \text{ output phase noise} = -46 \text{ dBc/Hz}$$

The resultant value of -46 dBc/Hz would make a very noisy PLL design.

Synthesizer Phase Noise

There are three sources of phase noise in a $\Delta\Sigma$ fractional-N synthesizer:

- Divider noise floor
- Multiplied Phase/Frequency Detector (PFD) noise floor
- Quantization noise of the $\Delta\Sigma$ modulator

The divider phase noise and the multiplied PFD noise floor normally contribute phase noise inside the loop bandwidth. The quantization noise normally occurs around 1 to 10 MHz offset from the carrier.

PFD and Divider Noise Floors

The SKY72300, SKY72301, and SKY72302 fractional-N synthesizers have internal VCO divider circuits. As such, it is difficult to discern the divider noise from the phase/detector noise floor. This Application Note refers to the combined divider and PFD noise floor as simply the PFD noise floor (-135 dBc/Hz for the SKY72300, SKY72301, and SKY72302 synthesizers). This occurs at point A in Figure 1.

As in the case of the crystal phase noise example, integer-N systems require the internal reference frequency to be very low to achieve the required step size. This causes the multiplied phase detector noise to rise inside the loop bandwidth. In this case, the noise floor is set by the noise floor of the PFD plus the $20 \log(N)$ factor.

Example 8:

Calculate the phase noise contribution of an integer-N synthesizer used to generate a 920 MHz output with a step size of 30 kHz.

The internal reference frequency is 30 kHz. The phase noise can be calculated using $20 \log(N)$:

$$\text{where: } N = \frac{F_{out}}{F_{ref}}$$

Therefore:

$$20 \log\left(\frac{920 \text{ MHz}}{30 \text{ kHz}}\right) = 89.7 \text{ dB}$$

The value of N is 30666.66. The 89.7 dB result is now added to the PFD noise floor.

If the PFD noise floor of the SKY72301 is -150 dBc/Hz at an internal reference frequency of 30 kHz, the resultant value would be:

$$-150 \text{ dBc/Hz} + 89.7 \text{ dB} = -60.3 \text{ dBc/Hz}$$

The result of -60.3 dBc/Hz would be the PFD noise contribution inside the loop bandwidth to the total phase noise of the PLL. To determine the total output phase noise, the multiplied noise contribution of the crystal oscillator must be added to this value.

Example 9:

Calculate the phase noise contribution of the SKY72301 fractional-N synthesizer used to generate a 920 MHz output with a step size of 30 kHz.

Since the SKY72301 uses fractional-N to achieve step size, the internal reference is not a small multiple of the required step size. The internal reference is determined by the crystal reference frequency divided by R (see the Crystal Oscillator Phase Noise paragraph below). Therefore, the crystal reference frequency and the value of the reference divider R need to be determined.

Assume a 20 MHz crystal and $R = 1$. With the reference divider $R = 1$, the internal reference frequency is equal to the crystal reference frequency of 20 MHz.

Calculate $20 \log(N)$ where: $N = \frac{F_{out}}{F_{ref}}$

Therefore:

$$20 \log \left(\frac{920 \text{ MHz}}{20 \text{ MHz}} \right) = 33 \text{ dB}$$

The value of N is 46. The 33 dB result is now added to both the PFD noise floor and the crystal oscillator noise floor.

If the PFD noise floor of the SKY72301 is -135 dBc/Hz while the crystal oscillator noise floor is -130 dB/Hz, the resultant phase detector noise contribution would be:

$$-135 \text{ dBc} / \text{Hz} + 33 \text{ dB} = -102 \text{ dBc} / \text{Hz}$$

and the resultant crystal oscillator noise contribution would be:

$$-130 \text{ dBc} / \text{Hz} + 33 \text{ dB} = -97 \text{ dBc} / \text{Hz}$$

The -102 dBc/Hz contribution of the PFD must be added to the -97 dBc/Hz noise contribution of the crystal oscillator, yielding an output phase noise at the VCO of -95.8 dB/Hz measured inside the loop bandwidth (note that if the reference divider was set to $R = 2$, then the crystal reference noise floor at the phase detector input would be 6 dB better, or -135 dBc/Hz).

This offers a significant improvement over the phase noise performance that an integer-N solution could provide (compare with Example 8). Also, the SKY72301 fractional-N solution offers a step size of 76 Hz as an added benefit.

$\Delta\Sigma$ Quantization Noise

Because Skyworks synthesizers use a $\Delta\Sigma$ modulator to achieve fractionality, the designer must be aware of the far-out quantization noise. This quantization noise occurs at point B in Figure 1. The quantization noise is only added to the feedback loop and not to the VCO noise. As a result, the quantization noise is attenuated by the loop filter.

The clock frequency of the $\Delta\Sigma$ modulator is set by the internal reference frequency where:

$$F_{Modulator} = F_{ref}$$

The formula is:

$$F_{Modulator} = \frac{F_{Xtal}}{R}$$

Example 10:

Calculate the clock frequency of the $\Delta\Sigma$ modulator if the crystal frequency is 50 MHz and $R = 2$:

$$F_{Modulator} = \frac{50 \text{ MHz}}{2}$$

This yields a 25 MHz $\Delta\Sigma$ modulator clock frequency.

Two factors are related to the internal reference that effect quantization noise. As illustrated by Figure 2, when the internal reference frequency increases, the amplitude of the quantization noise decreases. Increasing the internal reference frequency by a factor of 10 decreases the quantization noise by approximately 70 dB.

Also, as the internal reference frequency increases, the frequency at which the quantization noise occurs increases proportionally as well. Increasing the internal reference frequency by a factor of 10 increases the frequency of the quantization noise by 10.

These are two additional reasons for keeping the internal reference frequency high. Having a low internal reference frequency would significantly raise the quantization noise and also move it inside the loop bandwidth where it could not be attenuated by the loop filter.

VCO Phase Noise

The free running phase noise of the VCO is typically the dominant contribution to the total phase noise outside the loop bandwidth and sets the far-out phase noise of the PLL. This occurs at point C in Figure 1.

Inside the loop bandwidth, the VCO phase noise is attenuated by the loop filter. As the loop bandwidth increases, the VCO phase noise contribution inside the loop decreases (refer to Figure 3).

In a single loop PLL architecture, the VCO free running phase noise cannot be corrected outside the loop filter bandwidth. As a result, it is essential that VCO free running phase noise from about 100 kHz to 10 MHz be below the required system phase noise mask, or to correct for the VCO phase noise the loop filter bandwidth would have to be extremely large.

In a fractional-N synthesizer, the loop bandwidth can be much larger than in traditional synthesizers. However, if the bandwidth is too large, the crystal oscillator phase noise, synthesizer phase noise, and quantization noise contributions would be affected.

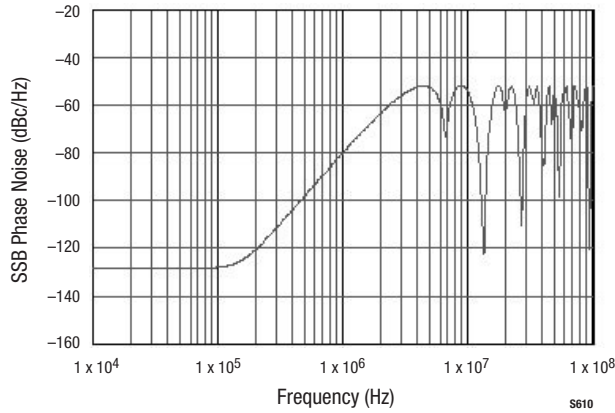


Figure 2. Typical $\Delta\Sigma$ Quantization Noise

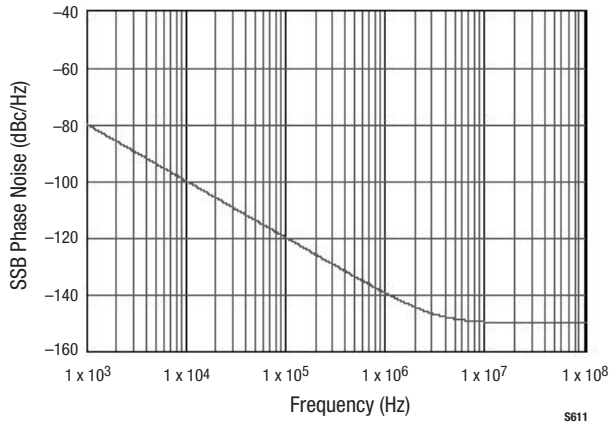


Figure 3. Typical VCO Free Running Phase Noise

Typical VCO free running phase noise is -150 to -140 dBc/Hz at a 10 MHz frequency offset and -120 to -110 dBc/Hz at a 100 kHz frequency offset.

When a VCO with poor phase noise is selected, the designer may be faced with a trade off: the VCO phase noise inside the loop against the crystal oscillator and synthesizer phase noise.

Loop Bandwidth

Loop bandwidth in this Application Note refers to the unity gain open loop bandwidth.

Larger loop bandwidths can be achieved with the SKY72300, SKY72301, and SKY72302 over traditional synthesizers due to the following reasons:

- Higher internal reference frequency. PLL synthesizer loop bandwidth is normally limited to 1/10 the internal reference frequency. Since the SKY72300, SKY72301, and SKY72302 can have an internal reference frequency as high as 25 MHz

while maintaining very fine step size, this is not a limiting factor.

- Crystal oscillator phase noise. The relatively small value of $20 \log(N)$, which is added to the crystal oscillator phase noise, reduces the PLL close-in phase noise.
- PFD noise floor. The multiplied noise floor of the PFD is below that of traditional synthesizers because the value of N is relatively small. This reduces the resultant synthesizer phase noise contribution inside the loop bandwidth.

Effects of Larger Loop Bandwidths

Increasing the loop bandwidth frequency has both positive and negative effects on the overall PLL performance.

Switching Time. The switching time of the PLL decreases as the loop bandwidth increases. To improve acquisition time the loop bandwidth should be increased.

The speed is approximated using the following equation:

$$Switching\ Time \approx \frac{10}{LoopBandwidth}$$

Example 11:

Using a 35 kHz loop bandwidth, and the above equation, switching time is equal to approximately 286 μs.

VCO Phase Noise. The VCO phase noise is improved by the loop filter only inside the loop bandwidth. Therefore, as the loop bandwidth is widened, the attenuation of the loop filter on the close-in VCO phase noise is improved. To improve the close-in VCO phase noise, the loop bandwidth frequency should be increased.

ΔΣ Quantization Noise. The loop filter attenuates the quantization noise which typically occurs around 1 to 10 MHz. Therefore, as the loop bandwidth increases, so does the quantization noise. To improve the quantization noise, the loop bandwidth frequency should be decreased.

Crystal Oscillator Phase Noise. The loop filter attenuates the crystal oscillator phase noise outside the loop. Therefore, as the loop bandwidth is increased, the point where the filter roll-off starts to attenuate, the crystal oscillator phase noise increases in frequency as well. To improve the crystal oscillator phase noise, the loop bandwidth frequency should be decreased.

Synthesizer Phase Noise. The loop filter attenuates the synthesizer phase noise outside the loop bandwidth frequency. Therefore, as the loop bandwidth is increased, the point where the filter roll-off starts to attenuate, the synthesizer phase noise

increases in frequency as well. To improve the synthesizer phase noise, the loop bandwidth frequency should be decreased.

Microphonics. Larger loop bandwidths help the PLL recover quickly from the effects of microphonics. The crystal oscillator is a piezoelectric device, which means that it is susceptible to short term phenomenon such as shock, vibration, and thermal earthquakes. Thermal earthquakes are caused by the mismatching of the coefficients of thermal expansion in the materials. This mismatch causes a buildup of stress that is periodically relieved by a sudden shift in mechanical alignment, which induces a mechanical shock.

Load Pulling of the VCO. With a larger loop bandwidth, the VCO will be less susceptible to any variations in the load. As a result, the synthesizer can correct the VCO more quickly. Otherwise, in a narrow loop, it is the reverse isolation of the VCO that is critical to protecting against load pull.

Figure 4 illustrates the measured phase noise performance of the SKY72300 PLL synthesizer. A typical performance crystal oscillator and VCO were used in this example:

- Crystal oscillator frequency: 24 MHz
- Internal reference frequency: 12 MHz
- PLL output frequency: 1200 MHz
- Loop filter bandwidth: 80 kHz
- Step size: 46 Hz

The loop filter has been optimized to 80 kHz to minimize the effect of the crystal, VCO, and quantization noise.

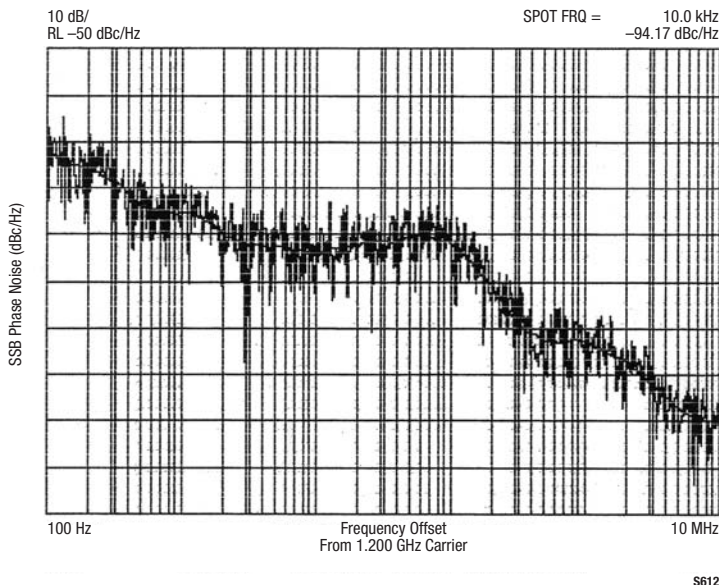


Figure 4. Measured Total Phase Noise Performance of the SKY72300 Main Synthesizer

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